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PTO/SB/08A (10-01)  
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Substitute for form 1449A/PTO		<b>Complete if Known</b>	
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (use as many sheets as necessary)		Application / Cnf. N .	Unknown 101 659 918
		Filing Date	September 11, 2003
		First Named Inventor	Jason H. Anderson
		Art Unit	Unknown 2825
		Examiner Name	Unknown Siek, V.
		Attorney Docket Number	X-1396 US
Sheet	1	of	1

OTHER - NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
VS		HALTER, JONATHAN P., "A Gate-Level Leakage Power Reduction Method for Ultra-Low-Power CMOS Circuits," IEEE Custom Integrated Circuits Conference, 1997, pages 475-478, IEEE, 3 Park Avenue, 17th Floor, New York, NY., 10016-5997.	
VS		YEAP, GARY, "Practical Low Power Digital VLSI Design," 1998, pages 59-72, available from Kluwer Academic Publishers, 101 Philip Drive, Assinippi Park, Norwell, Massachusetts, 02061	

Examiner Signature	WHE SIEK	Date Considered	3/23/05
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\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

<sup>1</sup> Applicant's unique citation designation number. <sup>2</sup> Applicant is to place a check mark here if English language Translation is attached.

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Sheet	1	of	1				

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Examiner Signature	VUTHE SIER	Date Considered	3/23/05
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